We claim:

1. A domino logic circuit comprising:

a pulldown circuit having a dynamic node;

a keeper connected to the pulldown circuit at the dynamic node; and

a source of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper.

2. The domino logic circuit of claim 1, wherein the body bias voltage is a reverse body bias voltage.

3. The domino logic circuit of claim 2, wherein the reverse body bias voltage is static.

4. The domino logic circuit of claim 3, further comprising a foot transistor for connecting the pulldown circuit to ground.

5. The domino logic circuit of claim 3, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

6. The domino logic circuit of claim 2, wherein source supplies the reverse body bias voltage such that the reverse body bias voltage alternates between two values.

7. The domino logic circuit of claim 6, further comprising a foot transistor for connecting the pulldown circuit to ground.

8. The domino logic circuit of claim 6, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

9. The domino logic circuit of claim 1, wherein the body bias voltage is a forward body bias voltage.

10. The domino logic circuit of claim 9, wherein the forward body bias voltage is static.

11. The domino logic circuit of claim 10, further comprising a foot transistor for connecting the pulldown circuit to ground.

12. The domino logic circuit of claim 10, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

13. The domino logic circuit of claim 9, wherein source supplies the forward body bias voltage such that the forward body bias voltage alternates between two values.

14. The domino logic circuit of claim 13, further comprising a foot transistor for connecting the pulldown circuit to ground.

15. The domino logic circuit of claim 13, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

16. The domino logic circuit of claim 1, wherein source supplies the body bias voltage such that the body bias voltage alternates between a first forward body bias voltage value and a second reverse body bias voltage value.

17. The domino logic circuit of claim 16, further comprising a foot transistor for connecting the pulldown circuit to ground.

18. The domino logic circuit of claim 16, wherein the pulldown circuit is connected to ground without an intervening foot transistor.

19. A source of an alternating voltage for biasing a keeper, the alternating voltage alternating between a first supply voltage and a second supply voltage, the source comprising:

an output connected to the keeper;

an input for receiving a clock;

a first supply voltage circuit connected between the first supply voltage and the output to supply the first supply voltage to the output;

a second supply voltage circuit connected between the second supply voltage and the output to supply the second supply voltage to the output;

a first transistor, connected to the clock without inversion, for selectively activating the first supply voltage circuit in accordance with the clock;

an inverter, connected to the clock, for outputting an inverted clock; and

a second transistor, connected to the inverter, for selectively activating the second supply voltage circuit in accordance with the inverted clock.

20. The source of claim 19, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the second supply voltage and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.

21. The source of claim 20 , wherein the output comprises a delay for supplying the first and second supply voltages to the keeper in a time-delayed manner.

22. The source of claim 21, wherein the delay is a non-inverting delay.

23. The source of claim 20, wherein the body bias generator further comprises a delay for delaying the clock to supply a delayed clock to the first and second transistors.

24. The source of claim 23, wherein the delay is a non-inverting delay.

25. The source of claim 19, further comprising a first node, a second node and a third node, wherein:

the first transistor is connected between the first node and ground and is gated by the clock;

the second transistor is connected between the second node and ground and is gated by the inverted clock;

the first circuit comprises a third transistor connected between the first supply voltage and the third node and a fourth transistor connected between the second supply voltage and the second node, the third and fourth transistors being gated in accordance with a signal from the first node;

the second circuit comprises a fifth transistor connected between the third node and the first node and a sixth transistor connected between the second supply voltage and the third node, the fifth and sixth transistors being gated in accordance with a signal from the second node; and

the output is connected between the third node and the keeper.